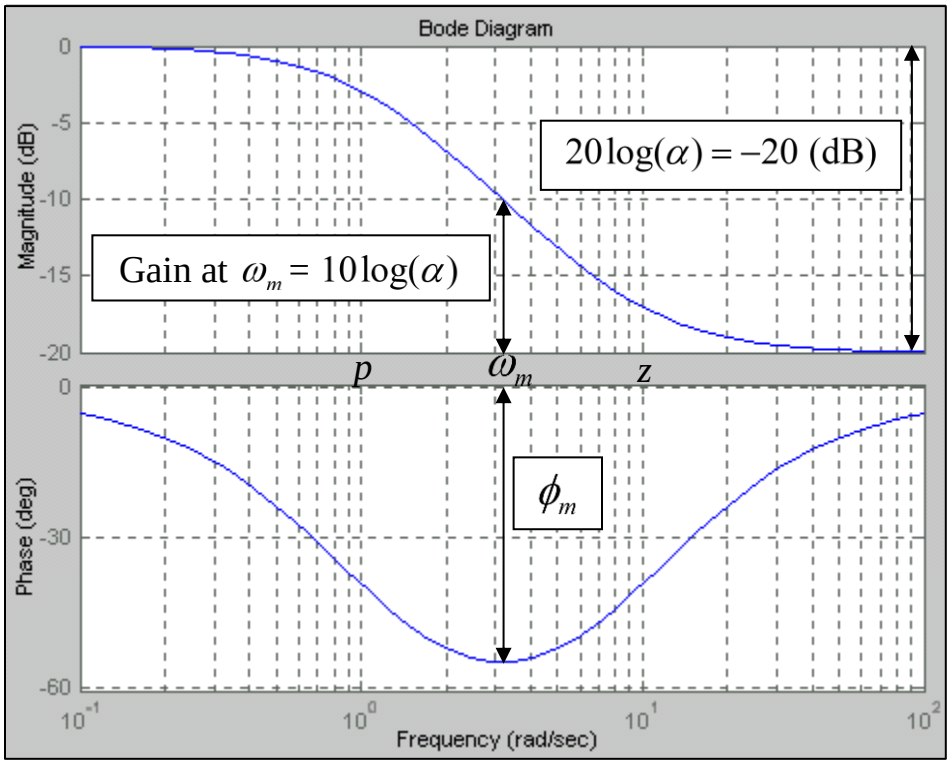
ME 4710 Motion and Control: Phase-Lag Compensator Design
Reference: Dorf & Bishop, Modern Control Systems, 10th Ed, Prentice-Hall, 2005.

Phase-Lag Compensator (PI type compensator)

- Transfer function of a phase-lag compensator: $G_c(s) = \alpha\left(\frac{s+z}{s+p}\right)$, where $|p| < |z|$
- The multiplier $\alpha = |p|/|z|$.
- Compensator ***decreases*** the gain of the system at frequencies above the location of the ***pole*** and ***decreases*** the phase of the system near the pole and zero locations.
- The Bode diagram of the phase-lag compensator $G_c(s) = \frac{1}{10}\left(\frac{s+10}{s+1}\right)$ is shown below.

Bode Diagram of the Example Phase-Lag Compensator



- The multiplier $\alpha = 1/10$, the ***logarithmic mean frequency*** is $\omega_m = \sqrt{|pz|} = 3.16$ (rad/s), the overall ***attenuation*** is $20\log(\alpha) = -20$ (dB), and the maximum decrease in phase (at the mean frequency) is $\phi_m = \sin^{-1}\left(\frac{\alpha-1}{\alpha+1}\right) = -54.9$ (deg).
- The ***main use*** of a phase-lag compensator is to ***decrease the steady-state error***. The ***cost*** is often to ***increase the system's rise*** and ***settling times*** (slower system).

Phase-Lag Compensator Design Using Bode Diagrams

- Find ***loop gain*** K required to satisfy the ***steady-state error requirement*** (if given).
- Evaluate the ***phase margin (PM)*** of the ***uncompensated system*** with the loop gain K to determine if proportional control is sufficient.
- Using the ***Bode diagram*** of the ***uncompensated system***, find the frequency where the phase margin requirement is satisfied (assuming this frequency is the zero-dB crossover frequency). ***Place*** the ***zero*** of the ***compensator at least one decade below this frequency***.
- Using the Bode diagram, determine the ***attenuation*** required to make the chosen frequency the new ***zero-dB crossover frequency***.
- ***Calculate*** α by setting the ***required attenuation*** (negative dB) equal to $20\log(\alpha)$.
- Calculate the ***pole location*** $p = \alpha z$, and define the compensator to be $G_c(s) = K\alpha\left(\frac{s+z}{s+p}\right)$.
- ***Check*** the ***phase margin*** of the ***compensated system*** to see if the desired value has been attained. If not, then decide on the additional phase required by the compensator, and repeat the steps above starting with the placement of the compensator zero.
- ***Simulate*** the time-domain performance.

Phase-Lag Compensator Design Using Root Locus Diagrams

- ***Target regions***: Set ζ and ω_n values for any complex poles (assuming they are all dominant and have no influence from zeros) to get a desirable percent overshoot and settling time.
- ***Examine*** the ***uncompensated RL diagram*** to see if the pole locations determined above can be met with only proportional control. Find the desirable root locations and the associated gain K and determine if the error requirement is satisfied. ***If not,*** choose $\alpha \approx K_{\text{uncompensated}} / K_{\text{desired}}$ and proceed.
- ***Add a real zero and a real pole*** to $GH(s)$ (usually close to the origin of the *s*-plane) modifying the root locus diagram to move branches into the target region. Changes the shape of the root locus diagram in predictable ways.
  - Can change the locations of real roots.
  - Separation between the pole and zero will ***move all asymptotes to the right***.
  - The location of any closed loop ***zeros*** may cause ***overshoot problems***.
- ***Simulate*** the time-domain performance.